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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,011	Applicant(s) BARTENSTEIN ET AL.	
	Examiner R. Stephen Dildine	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-25* is/are allowed.

6)☒ Claim(s) *1,8,9 and 26* is/are rejected.

7)☒ Claim(s) *2-7 and 27-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Archibald et al. A comparison of these claims with the disclosure of Archibald et al. follows:

Applicant's Claim 1	**Archibald et al.**
A method of testing a semiconductor device having a memory	"A method, computer readable medium, apparatus and RAID controller for performing nondestructive write testing is disclosed" Abstract, first sentence.
comprising: selecting a portion of said memory;	"For data storage devices divided into sectors" Abstract, second sentence.
testing said selected portion of said memory	"however, it will be appreciated that the media surface scanner 109 may be controlled so as to scan only selected portions of the media, to skip particular portions of the media, to scan selected portions of the media more or less frequently than other portions, or directed to scan according to other predetermined or programmatically constrained rules" ¶ [0023]
designating said selected portion of said memory as a designated memory in response to an acceptable testing result	"Desirably, the media surface scanner 109 will traverse all sectors on the media so that any media defect wherever located can be identified" ¶ [0023] in other words, in response to an acceptible testing result, a sector is designated as 'not identified'
and storing data in said designated portion of said memory for retrieval at a later time	"If no errors are detected during the read phase of the test (step 306), the controller 100 will write back the read data to the sector (step 304)" ¶ [0026]
Applicant's Claim 8	**Archibald et al.**
further including sending said data to a tester	"the number and pattern of errors are such that they can be corrected or recovered using the normal error detection and correction procedures" ¶ [0025]

Claims 1, 9 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Adams et al. (5,912,901). A comparison of these claims with the disclosure of Adams et al. follows:

Applicant's Claim 1	Adams et. Al
A method of testing a semiconductor device having a memory	"With reference now to FIG. 1, there is illustrated a conventional closed-loop testing apparatus for an integrated circuit memory" column 1, lines 35-37
comprising: selecting a portion of said memory;	"As will be understood by those skilled in the art, memory array 32 comprises a number of individual memory cells which are each accessed for reading or writing data by selecting particular word and bit lines" column 3, lines 6-9; therefore, the selected portion of said memory is an individual memory cell.
testing said selected portion of said memory	"BIST 12 applies internally generated test data and address data to memory array 18 and compares output data read out from memory array 18 with expected data" Column 1, lines 45-48
designating said selected portion of said memory as a designated memory in response to an acceptable testing result	"In response to a discrepancy between the output data and the expected data, BIST 12 indicates that a failure within memory array 18 has been detected by driving diagnostic output (DGO) signal 20 high" column 1, lines 48-51; therefore, if there is an acceptable testing result, designated memory would be indicated by diagnostic output (DGO) signal 20 low.
and storing data in said designated portion of said memory for retrieval at a later time.	If a memory is determined to be error free, it is notoriously well known to those skilled in the art at the time of applicants' invention to use said memory for data storage and this is implied in the disclosure of Adams et al. since his invention is assumed by the patenting process to be useful.

Applicant's Claim 9	Adams et. Al
The method of claim 1, wherein said data is generated by ABIST or LBIST	"or array built-in self-test (ABIST) circuits and will hereinafter be referred to generically as BIST", column 1, lines 33-35
Applicant's Claim 26	**Adams et. Al**
a memory	"With reference now to FIG. 1, there is illustrated a conventional closed-loop testing apparatus for an integrated circuit memory" column 1, lines 35-37
an ABIST engine adapted to test said memory	or array built-in self-test (ABIST) circuits and will hereinafter be referred to generically as BIST
an interface adapted to send test data to and receive test data from a designated portion of said memory	"BIST 12 applies internally generated test data and address data to memory array 18 and compares output data read out from memory array 18 with expected data" Column 1, lines 45-48

Claims 2-7 and 27-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-25 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brunelle, Lee et al. and Tanabe et al. are all cited to show a method of testing a semiconductor device having a memory, comprising: selecting a portion of said memory; testing said selected portion of said memory; designating said selected portion of said memory as a designated memory in response to an acceptable testing result; and storing data in said designated portion of said memory for retrieval at a later time. Ternullo is cited to show a memory test apparatus for use with memory having a plurality of outputs, including a built-in, self-testing (BIST) test state machine having a plurality of address outputs; a plurality of multiplexers controlled by the address outputs of the test state machines; and means for testing the plurality of outputs of the memory based on the address outputs of the test state machine, wherein the plurality of outputs of the memory are input to the plurality of multiplexers and a number of outputs tested simultaneously is less than a total number of outputs of the memory. TDB-ACC-NO: NNRD439133 and Matsumura are cited to show BIST memory testing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. Stephen Dildine whose telephone number is 703-305-5524. The examiner can normally be reached on M, Tu, Th, F 5:55 am to 4:25 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

R. Stephen Dildine
Primary Examiner
Art Unit 2133

R. Stephen Dildine